A Method for Digitally Simulating Shorted Input Diode Failures

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Most existing digital fault simulators can simulate only a somewhat restrictive class of failures; namely, stuck at "1" and stuck at "0" faults. The problem seems to be the lack of techniques for properly treating the effects due to "backward propagation" of errors. This paper describes a method for illustrating how shorted input diode failures, which previously could not be simulated, can be handled by digital methods. The method is applicable to all other modes of failures describable by truth tables or Boolean expressions. Furthermore, we examine the problem of circuit oscillations caused by backward propagating errors. We conclude that failure induced oscillations can only occur under very restrictive conditions.

I. INTRODUCTION

Digital fault simulation is the method of predicting the behavior under failure of a logical circuit by a computer program: that is, the use of a computer to aid in computing the output(s) of a logical circuit for a given input or a given set of inputs.[1] One of the drawbacks of existing digital fault simulators is that the class of failures capable of being simulated is somewhat restrictive. Most simulators, such as IBM's Saturn Fault Simulator and Seshu's Sequential Analyzer (see Refs. 2 and 3) consider only those failures which cause some connection in the logic circuit to appear stuck at "1" (stuck-at-1)or stuck at "0" (stuck-at-0).* Shorted input diode failures of low level logic (LLL) gates, for example, therefore cannot be simulated because they are not describable by stuck-at-1 or stuck-at-0 types of faults.

In this paper we describe a method illustrating how shorted input diode failures can be simulated digitally, using a technique somewhat

* Other common assumptions made are (*i*) the fault-free circuit is well behaved; (*ii*) the class of faults considered is finite and nonintermittent; and (*iii*) the single-fault assumption is used.

different from the conventional approaches. The method can be easily extended to simulate other types of failures describable by means of truth tables or Boolean expressions. The oscillatory circuit behavior resulting from "backward propagation" of errors is also analyzed.

II. NATURE OF THE PROBLEM

The effectiveness of any simulator depends largely on how accurately the structure and the behavior of a physical model can be described by the model used in the simulator. In the case of a fault simulator, one must ascertain that the presence of any fault in the physical model can be accurately reflected in the simulator by appropriately changing the structural description of the simulated model. Experience has shown that stuck-at-1 and stuck-at-0 faults are quite common in most logic circuit realizations, and that these faults can be conveniently represented in the simulator by a technique called the failure-injection-word approach (see Ref. 3).† However, for shorted input diode failures, and possibly for many other unforeseen integrated circuit failure modes, the failure-injection-word approach will no longer be applicable. Some means for digitally simulating faults other than those of stuck-at-1 or stuck-at-0 types must therefore be devised.

Consider the three-NAND low level logic gate circuit shown in Fig. 1 and investigate, respectively, the possible malfunctions of this circuit caused by (*i*) shorting diode D_1 between input terminal *a* and transistor Q1 and (*ii*) shorting diode D_2 between transistors Q1 and Q2.

Case (*i*): When D_1 is shorted, point *x* will always be at the same potential as point *a*. Whenever the potential at terminal *b* goes "low," the level at point *x*, and therefore terminal *a*, will also go "low." However, since there is no fanout at terminal *a*, other gates will not be affected. Furthermore, it can be easily verified that for all combinations of inputs at terminals *a* and *b*, the output of Q1 remains normal; no trouble symptoms will be propagated to other parts of the circuit. Hence, we may conclude that the shorting of diode D_1 does not affect the operation of this circuit.

Case (*ii*): When diode D_2 is shorted, we can verify that no erroneous signals will be observed at the output terminal of Q2. However, because of the presence of fanout at point *y*, whenever the potential level at terminal *c* goes "low," the level at point *y* will also go low, causing a possible erroneous output at terminal *t*. Thus although the fault is

† Other methods of analysis can be found in Refs. 4 and 5.

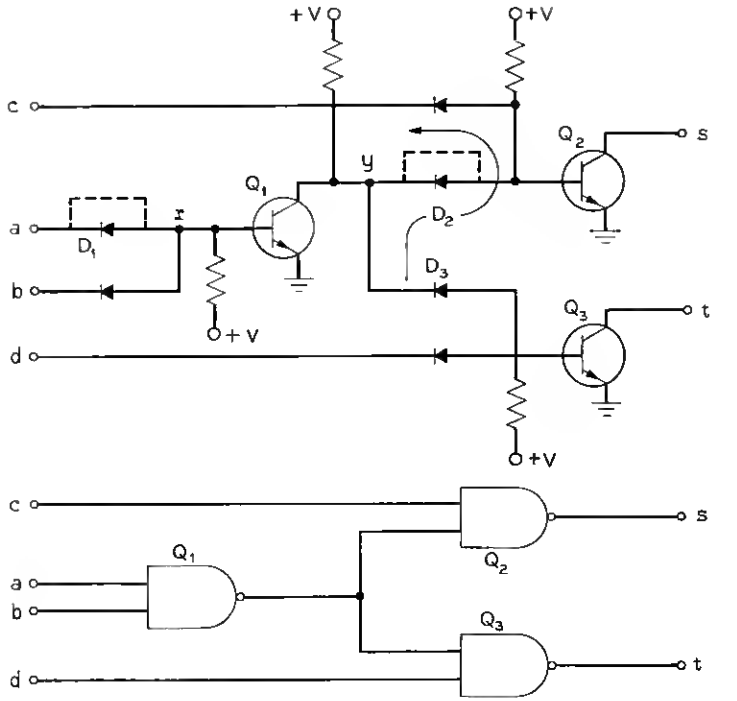


Fig. 1 — A logic circuit with the NANDs.

associated with gate Q2 (from a logic viewpoint), trouble symptoms caused by the fault are not observable at the output of Q2, but are observable at the fanout gate Q3. This is tbe "backward propagation" of errors. In the case where there is fanout to many gates, all these gates would be affected.

At this point, we may summarize that the behavior of a logic circuit under a shorted input diode failure is inconsistent. If the input terminal of the faulty diode has no fanout, the circuit outwardly behaves in the same manner as a fault-free circuit; if the input terminal has fanout, malfunctions then propagate to other fanout gates but do not affect the gate to which this faulty diode is connected. At first glance it may appear that faults, such as shorted input diode failures, causing errors propagating backwards are difficult to analyze and therefore unsuitable for digital simulation. However, further study shows that if the nonstuck at "1" and nonstuck at "0" types of failures

are describable by truth tables, a systematic procedure can easily be devised to cope with these situations.

III. A SOLUTION

Consider a three-input NAND gate with input terminals x, y, z, and output terminal Q. As previously mentioned, any time an input diode is shorted, the output of a NAND behaves in the same way a fault-free NAND behaves. However, if any one of the input terminals goes "low," the terminal associated with the shorted diode will also go "low." The condition can be described by constructing a truth table for the faulty three-input NAND as shown in Table I. Part (*i*) enumerates all the input combinations; part (*ii*) shows the effect of input diode x shorted on all input and output terminals. Equivalently, by realizing Table I, we may represent the condition using the following expressions:

$$\left.\begin{aligned} Q_{NAND}(x \text{ shorted}) &= (xyz)' \\ x(x \text{ shorted}) &= Q' \end{aligned}\right\}. \tag{1}$$

Equation (1) indicates that to simulate a shorted input diode fault, say at terminal x, of a NAND gate, one first computes the output Q as usual; one then changes the logic state of terminal x to be the complement of the gate output Q. This must be done before other gates which are fanouts from terminal x are simulated. In other words, simulation is accomplished in two passes (over the gate), rather than in one pass, as was the case with the failure-injection-word approach.

In order to avoid the complication resulting from backward error

TABLE I—TRUTH TABLE REPRESENTATION OF SHORTED INPUT DIODE CONDITIONS FOR NAND GATE

(*i*) Inputs			(*ii*) Diode x shorted			
x	y	z	x	y	z	Q
0	0	0	0	0	0	1
0	0	1	0	0	1	1
0	1	0	0	1	0	1
0	1	1	0	1	1	1
1	0	0	⊡	0	0	1
1	0	1	⊡	0	1	1
1	1	0	⊡	1	0	1
1	1	1	1	1	1	0

propagations, all gates in a logic circuit must be organized by "level," as was done in the conventional approach.[3] By "level" we mean that all primary inputs and feedback inputs (in the sense of Huffman, see Ref. 6) are of level zero; a gate is of level n if all the inputs at the gate are of level $n-1$ or less and at least one input is of level $n-1$. To begin simulation, we apply a particular combination of primary inputs and feedback inputs to all gates of level 1; we compute the logic states of gate outputs and then all input terminals that have fanout using equation (1) to reflect the shorted input diode failure mode (of NAND gates). We proceed in a similar fashion to compute the outputs of all gates of level 2, all gates of level 3, and so on.

Notice that faults can still be simulated several at a time if, as in the failure-injection-word approach, each fault is represented by a "bit" of a computer word and these bits are properly packed. Finally, we resimulate the whole circuit once more, in a way similar to the failure-injection-word approach. The reason for resimulating the circuit is that there are gates of level j whose input(s) may be fed from some gate of level k, and $j > k$ (see Fig. 2). When gates of level j are being simulated, the states of all gates of lower levels, such as those of level k, have already been computed. Thus, to insure that the effect of shorted input diode fault(s) at any level properly propagates backward to gates of lower level(s), such as shown in Fig. 2, another pass must be computed over the whole circuit to obtain the correct results. With this approach, backward error propagations resulting from fanouts can be properly handled.

The technique can easily be extended to simulate the same failure for other types of gates, as long as they are describable by Boolean expressions. The truth tables describing shorted input diode failures for AND and OR gates are given in Table II.*

The equivalent Boolean expressions for Table II are

$$\begin{aligned} Q_{AND}(x \text{ shorted}) &= x \cdot y \\ x(x \text{ shorted}) &= Q_{AND} \end{aligned} \tag{2a}$$

and

$$\begin{aligned} Q_{OR}(x \text{ shorted}) &= x \\ y(x \text{ shorted}) &= x \cdot y. \end{aligned} \tag{2b}$$

* We assume the driving element is much more potent in the zero-going (positive logic) direction than in the positive-going direction, as in the case of the collector of a saturating n-p-n transistor with resistive pull-up.

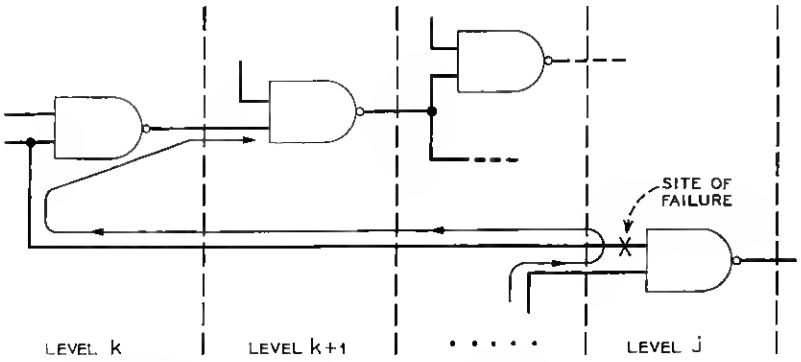


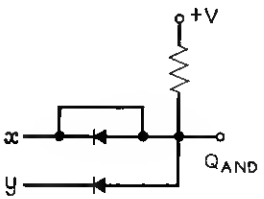
Fig. 2 — Backward propagation of error resulting from shorted input diode failure.

It is apparent that the truth table or Boolean expression approach, for describing failure modes of gates for digital simulation, can also be used to represent stuck-at-1 and stuck-at-0 faults. It should also be mentioned that methods for handling certain nonstuck at "1" and nonstuck at "0" types of failures have been treated by Roth.[5] However, the technique for constructing the singular cover of the faulty gate(s) for shorted input diode types of failures is not discussed.

TABLE II — TRUTH TABLE REPRESENTATIONS OF SHORTED INPUT DIODE CONDITIONS

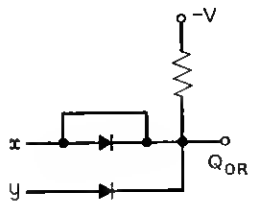
2—Input AND

(i) Inputs		(ii) Diode x shorted		
x	y	x	y	Q_{AND}
0	0	0	0	0
0	1	0	1	0
1	0	◎	0	0
1	1	1	1	1



2—Input OR

(i) Inputs		(ii) Diode x shorted		
x	y	x	y	Q_{OR}
0	0	0	0	0
0	1	0	◎	◎
1	0	1	0	1
1	1	1	1	1



IV. INDUCED OSCILLATIONS

In some cases the backward propagation of errors can produce oscillations in a normally well-behaved circuit. For example, consider the exclusive-OR circuit (realized in terms of NAND gates) as shown in Fig. 3. With inputs $a = 1$, $b = 1$ and the input diode from b to NAND gate Q2 shorted, the error will propagate around the "loop" Q2 $\rightarrow$ b $\rightarrow$ Q1 $\rightarrow$ Q2 and thus makes Q1 oscillate, which in turn causes Q4 to oscillate.† At first glance, it seems that the problem presented by induced oscillation can be extremely complicated. However, the situation is still manageable.

One of the necessary conditions under which oscillations caused by backward propagation of errors may result is that the site of failure be located at a place where reconvergent fanout paths converge. Reconvergent fanout paths are defined to be those fanout paths of some gate of level k that reconverge at some gate of level $k + i$ ($i \geq 1$). This is because if there are no reconvergent fanout paths in a circuit, no "loop" can be formed when an input diode of any gate is shorted. Consequently, no oscillation is induced. Thus in circuits having no reconvergent fanouts, the two-pass technique accurately simulates the circuit behavior.

Now, suppose a circuit has some reconvergent fanout paths. Consider gate Q_a of level k whose fanout paths reconverge at some gate Q_b of level $k + i$ (see Fig. 4). Call the number of gates traversed by a reconvergent fanout path from Q_a to Q_b the degree of that path. It is not difficult to see that another necessary condition for the existence of induced oscillation (caused by a shorted input diode at Q_b) is that there is at least one path of degree zero from Q_a to Q_b. In other words, if every reconvergent fanout path from Q_a to Q_b is of degree one or greater, errors at Q_b cannot propagate backwards to Q_a, as they will be "blocked" by gate(s) lying in paths between Q_a and Q_b. Consequently, induced oscillation is not possible under these conditions.

Furthermore, in the case where one of the reconvergent fanout paths from Q_a to Q_b is of degree zero, oscillation will not result if there is no "sensitized" path(s), under the given input condition, from Q_a to Q_b.[4,5] This is because if there are no sensitized path, errors originated at Q_b and propagated backwards to Q_a will not be able to propagate forward to Q_b. Even in cases where there is some sensitized path(s), if the number of inversions of logic signal along the sensitized path(s), from

† Physically, if the temporal length of the loop is short with respect to circuit operation time, oscillation will not occur.

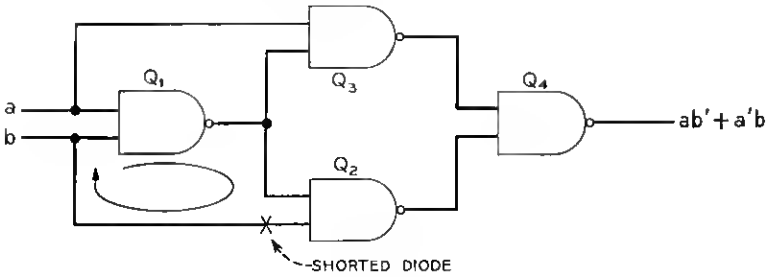


Fig. 3 — An exclusive-OR circuit.

Q_a to Q_b is even, no oscillation will result either, since all those inputs of Q_b belonging to the reconverging fanout paths will have the same parity (as that of the particular input where the diode is shorted).

As a result, we conclude that oscillations caused by backward propagation of errors can occur, but only under a very restrictive set of conditions. In the case of shorted input diode failures, oscillation can occur if (*i*) the site of failure is located at a place where some reconvergent fanout paths converge, and is on at least one reconvergent fanout path of zero degree (see Fig. 4), and (*ii*) for the given input condition, the number of inversions of logic signal along some sensitized, reconvergent, and gain producing path(s) terminating at the site of failure is odd.

There are a number of ways to handle the problem presented by induced oscillations. One method is to first locate, from the circuit description, all groups of reconvergent fanout paths in which at least one

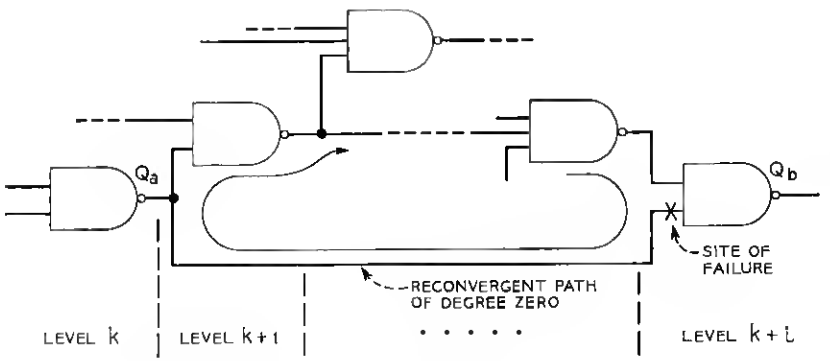


Fig. 4 — A circuit with a reconvergent path of degree zero.

path is of degree zero. Then, by flagging those gates that are members of these groups, we can repeatedly interrogate those flagged gates during simulation runs to determine whether there is any oscillation. As multipass simulation can be very time consuming for large circuits, it may not be economically justifiable in view of the stringent set of constraints that must be met for oscillations to occur. The other method is to modify the logic design by eliminating all zero-degree reconvergent fanout paths. This can be done by either inserting a gate in series in the zero-degree path, or by adding a gate in parallel at the site of fanout to replace the zero-degree path, or by using some other design tricks. The choice of method depends largely on the cost of its implementation and the reliability requirement of the particular application.

V. CONCLUSION

A method has been described illustrating how shorted input diode failures, which previously could not be simulated by digital fault simulators, can be handled by digital methods. It has also been shown that the method can be easily extended to simulate all other modes of failures, including stuck-at-1 and the stuck-at-0 types of faults, describable by truth tables or Boolean expressions.

Furthermore, it has been pointed out that the backward propagation of errors can sometimes produce oscillatory behavior in a normally well-behaved circuit. Failure induced oscillations, although occurring only when a rare combination of conditions exists, can nevertheless complicate the simulation process, and make the circuit behavior unpredictable. It is therefore desirable to eliminate these problems by modifying the logic circuit during the design stage.

VI. ACKNOWLEDGMENT

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REFERENCES

1. Manning, E. G., and Chang, H. Y., "A Comparison of Methods for Simulating Faults of Digital Systems," Digest of the First Annual Computer Conf., Chicago, Illinois, September 1967, pp. 10–13.
2. Hardie, F., and Suhocki, R., "Design and Use of Fault Simulation for Saturn Computer Design," IEEE Trans. Elec. Computers, *EC-16*, No. 4 (August 1967), pp. 412–429.

3. Seshu, S., and Freeman, D. N., "The Diagnosis of Asynchronous Sequential Switching Systems," IRE Trans. Elec. Computers, *EC-11*, No. 4 (August 1962), pp. 459–465.
4. Armstrong, D. B., "On Finding a Nearly Minimal Set of Fault Detection Tests for Combinational Logic Nets," IEEE Trans. Elec. Computers, *EC-15*, No. 1 (February 1966), pp. 66–73.
5. Roth, J. P., "Diagnosis of Automata Failures: A Calculus and a Method," IBM J. Res. Development, *10* (July 1966), pp. 278–291.
6. Huffman, D. A., "Synthesis of Sequential Switching Circuits," J. Franklin Inst., *257*, Nos. 3 and 4 (March and April 1954), pp. 161–190, 275–303.